EDN's Hands-On
SMT Project—Part 5

Automated testing of SMT pc boards

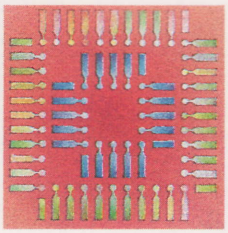
When they came off the manufacturing line, our boards didn't work at all. To find out why, we handed them to ATE engineers, who built a test fixture, wrote and debugged a test program, and found the manufacturing defects on each board. The information they provided allowed us to repair the defects and eventually produce a working SMT assembly.

It's no fun gazing at a dead pc board, and it's not very productive either, so we hustled some blank pc boards and completed assemblies to Hewlett-Packard's Manufacturing Test Division (HP MTD) in Loveland, CO. We started this project without a test plan: With an optimism typical of most design engineers, we expected the boards to work immediately after we assembled them. At this point in the project, we felt very fortunate that Hewlett-Packard had agreed to help us.

HP designed and built a test fixture to mate our cir-

Steven H Leibson, *Regional Editor*

Illustration by Michael Young



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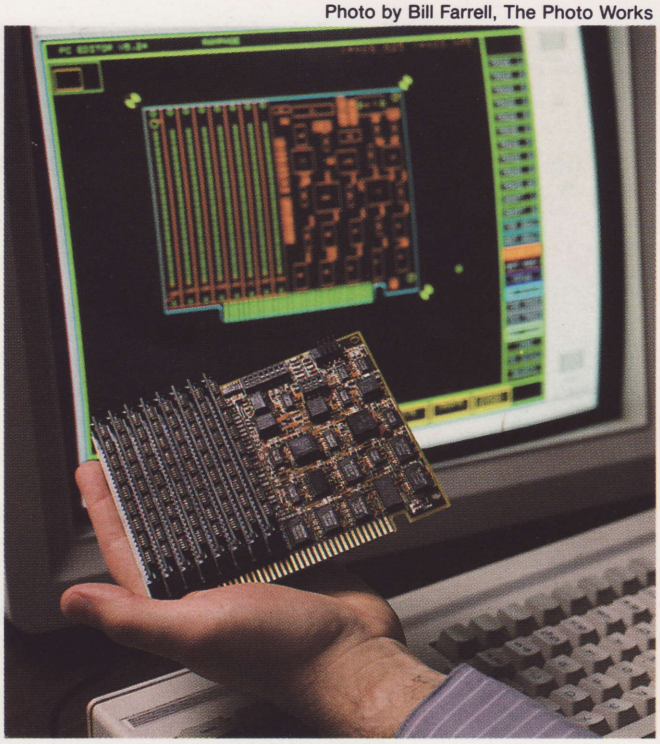


Our finished assembly exactly matched the model we created using the Cadnetix workstation. In-circuit testing and a little rework to repair manufacturing defects produced a working circuit board.

cuit board to the company's HP3065 in-circuit, board-test system. A new product—the HP44203 Simplate test fixture—served as the starting point for our custom fixture. With the Simplate, tooling pins and test probes are mounted on only one plate, eliminating the tolerance accumulation of the more conventional 2-plate approach (see **box,** "Test fixtures for SMT Assemblies"). HP estimates that the fixture it built for EDN's project board cost $2800 in time and materials.

MTD assessed our design and considers it to be very testable because every circuit node intersects at least one via that can be probed from the back of the pc board. In fact, the company uses our project board to show its customers how to design a testable SMT assembly. HP's Simplate test fixture accommodates both 100-mil and 50-mil test probes, but out of 192 testable nodes on the EDN SMT project board, only seven required the use of 50-mil probe pins. HP used 100-mil probes for the other 185 nodes. Although 50-mil pins are available for tight board designs, those probes cost more and fail more frequently than 100-mil probes.

Because we had not filled the vias on our board with solder during assembly, the test fixture's vacuum was not adequate to pull the pc board down onto the test probes. Air leaked through the open vias, reducing the suction. Had we forseen this, we would have taken steps to fill the vias during the wave soldering of the memory sockets. HP solved this problem by building a plastic top cover for our test fixture.

A top cover gets in the way

The top cover incorporates adjustable push pins to press the pc board against the test probes. The cover also prevents contaminants from being sucked through the pc board's vias and into the test fixture by the vacuum. Although the electrically passive top cover costs far less than a cover containing probes for 2-sided probing, it still increases test costs directly through additional fixture complexity and indirectly through increased test cycle time. Each time a board is tested, the operator must open the cover, install the pc board on the fixture, close the cover, and

Test fixtures for SMT assemblies

Hewlett-Packard's Manufacturing Test Division (HP's MTD) took our SMT assembly, designed and built a custom test fixture for our pc board, and wrote the test that identified all of the manufacturing defects on our completed boards. MTD's application center used the company's new Simplate test fixture, designed for its HP3065 in-circuit board-test system, to test our board. HP specifically designed the Simplate for the tighter tolerances encountered in testing SMT assemblies.

Kris Jones, the product marketing engineer who supervised the fixture construction for us at MTD, says that, compared with 2-plate fixtures, the Simplate fixture provides five times better repeatability for contacting our small, 36-mil vias. She also asserts that if MTD had used a conventional 2-plate fixture, the lack of precision in the fixture could have caused as much as 9% of our assemblies to fail the in-circuit test because the fixture's probes would have failed to contact our small vias.

activate the test. In addition, the cover prevents an operator from activating the switches on the board during the test. For this reason, we did not thoroughly test the switches on the in-circuit tester.

HP personnel determined the locations for the test probes on our fixture by "bomb-sighting" the vias on our pc board using an optical digitizer. This approach allowed the builders to create a fixture that matched the fabricated pc board rather than the theoretical model produced by the Cadnetix workstation. It was also easier for HP to manually digitize a fabricated pc board than to translate the pc-board design data from the Cadnetix workstation's format into HP's format. This phase represented yet another point during this project when people manually transferred information from one computer system to the next. We look forward to the day when a universal interchange format, like the developing EDIF standard, makes all of these manual transfers unnecessary.

The plate drilling and the wiring of the fixture required about one week. After the fixture was ready, HP's test engineers became involved with the project. Mitch Killmon and Jim Benson developed the test program for EDN's project board. The first step, transcribing the schematics, required about two and a half days. Note that once again the Cadnetix files weren't used: The test engineers effected the schematic transfer manually.

The HP3065's automatic test generator (ATG) took the first crack at creating a test program by using standard device models for most of the parts on our board. The PLDs and PROMs required custom models provided by HP MTD's application center. At this point, the two test engineers sat down to make the test work. Right off the bat, some of the tests created by the ATG required modification. Because the HP3065 tester overdrives IC outputs during some tests, the test engineers broke up long tests into several shorter tests to prevent the tester from damaging the components on our board.

We placed these engineers in an

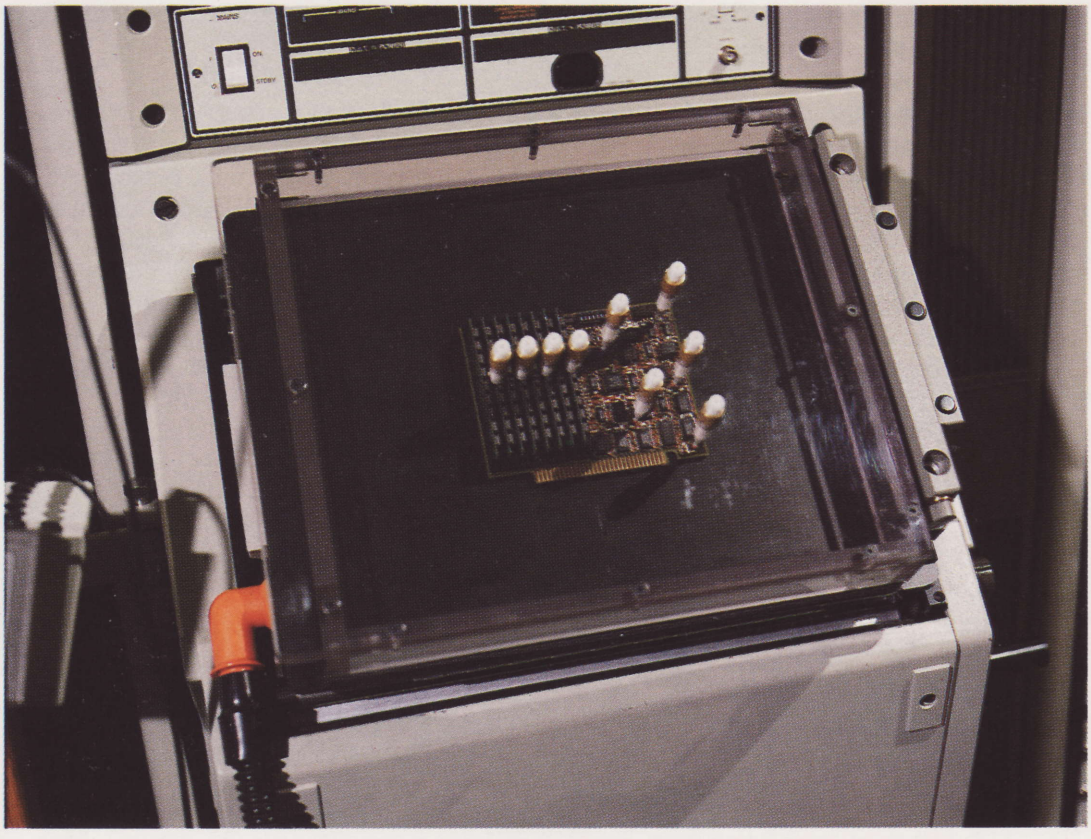
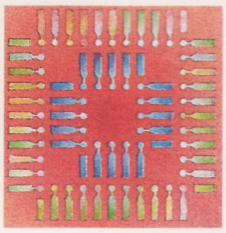


Photo by Gary Guerriero, Hewlett-Packard

Because we left the vias in our board unplugged, the in-circuit tester's vacuum system could not draw our board down onto the bed-of-nails test fixture. Therefore, Hewlett-Packard designed a top cover for the fixture that mechanically pushed the board onto the test probes.



unusual situation: We had no "golden" (known good) board. Test failures could be caused by the manufacturing defects on our boards, by bad components, or by an improper test. Without a golden board, the engineers had to consider all three possibilities. They took each failure on a case-by-case basis and found that failures caused by real defects were relatively easy to identify. The test ran completely after three days of debugging.

Of those three days, the test engineers spent an entire day chasing a problem with the dynamic-RAM test. The test indicated intermittent failures in the memory array, and the failures appeared to be position sensitive.

Photo by Gary Guerriero, Hewlett-Packard

The two test engineers from Hewlett-Packard, Mitch Killmon (left) and Jim Benson, took the in-circuit board-test program created by the HP3065's automatic test generator and massaged it into a working test.

Ultimately, the culprit turned out to be the RAMs' need to be cycled eight times after powering up before they would operate properly. Adding a 1-line cycling routine at the beginning of the RAM test made all of the intermittent problems disappear.

The test engineers also noticed that the project board's power-to-ground capacitance jumped when they plugged the SIP memory modules into their sockets. Although not visible and not shown on the schematic, a bypass capacitor resides beneath each dynamic-RAM PLCC on the SIP memory module, so the pc board's bypass capacitance more than triples when all eight modules are in place. The test engineers added a little more code to the test program to accommodate the extra bypass capacitance. HP estimates that the cost for creating this test was approximately $5800.

When the test was ready, we brought all of the assemblies to HP for testing. The test quickly identified open connections, bad components, and wrong components. We then took these defective boards down to HP's rework area and repaired the manufacturing flaws. Then we took the assemblies back up to the tester and looked for more problems. By the end of the day, we had six boards that passed the test. We rushed these boards back to our office, plugged them into an IBM PC for a system test, and watched all of the boards once again fail to pass the computer's power-on self test.

This situation put us in a bad position. The HP3065 tester had blessed these boards. That meant that, as far as the ATE was concerned, the assemblies matched our schematic. We didn't know if we had incorrectly transcribed the schematic (although we and HP had triple checked our work), if we had caused a timing problem to appear through the use of SMDs (they're usually faster than equivalent through-hole parts), or if the documentation we had received from AST Research was wrong.

Sorry, wrong number

At this point we boxed two of the tested assemblies and copies of all of the engineering documentation we had generated and shipped the package off to AST. We soon had the answer to our problem. Both of the PROM listings we'd received from AST were wrong. They were down-level versions used on the prototype Rampage! board and didn't match the production version of the circuit design that we had used. AST sent us new PROM listings to

solve the predicament.

Next, we needed to program some new PROMs, but of course we had used up our entire stock of devices to assemble our boards. Once again, we were gently reminded to always acquire three times more prototyping stock than we think we'll need. We made some phone calls and received the required parts in a couple of weeks. Then we visited Cadnetix to borrow the company's device programmer once again, and we burned the new codes into the PROMs. We journeyed back to HP MTD, where a repair technician carefully removed the old PROMs and soldered the freshly programmed parts onto the boards.

Avoid rework like the plague

Each PLCC PROM package required about 15 minutes to replace, using some fairly sophisticated rework equipment. We were struck by the slowness of the repair procedure and recalled all of the times during this project that one expert or another had told us to get our process right the first time. Rework on an SMT board is costly in terms of time, personnel, and equipment. You don't have to watch too many of these SMT repair jobs to realize the importance of making sure, in every possible way, that your board is optimized for manufacturability. Although the 10 pc boards in our prototype run had several manufacturing flaws, we feel that we understand the causes of those defects and could avoid them in a production environment because of the experience gained during this project.

With the new components installed, we placed the boards back on the HP3065 tester and verified the repairs. Then, we returned to our office and attempted to run the refurbished boards in our PC. Once again it was no dice. Another call to AST gained us one more piece of information: We still didn't have the production PROM codes on our boards. AST had written new PROM codes for us, trying to compensate for perceived differences between AST's schematic and ours.

Success at long last

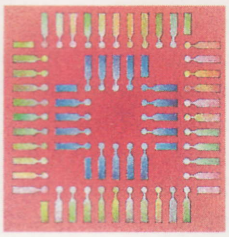
At this point, AST asked that we send the boards to them and took responsibility for making our assemblies work. We gladly shipped the company two more assembled pc boards. It turned out that the new PROMs required some nonstandard switch settings. With those settings, our boards completed all system tests with flying colors and ran like the Rampage! clones they were supposed to be. We had achieved our goal: We had produced a working, SMT version of a through-hole product.

Photo by Gary Guerriero, Hewlett-Packard

Even with the proper equipment, rework and repair of SMT boards require substantial amounts of time. We spent about two hours replacing two PLCCs on each of eight circuit boards at Hewlett-Packard's Manufacturing Test Division.

In the conversion process, we reduced the Rampage! board's size by approximately 60%. The SIMMs allowed us to shrink the real-estate consumption of the memory array on the board by 74%. Although more exotic SMT techniques like placing components on both sides of the board would have allowed us to further reduce the size of our board, we achieved our goal of creating a board that fit into a PC's short slot without resorting to such higher-cost approaches.

Since we completed the construction of the project board, many of the people who helped us



on the project have had a chance to evaluate the finished product and the worthiness of our design. We did a lot of things right. The training we received at the beginning of the project paid off well. The EDN SMT project board has the two characteristics we strived to attain: manufacturability and testability.

We did not do everything right, however. John Maxwell at AVX (Colorado Springs, CO) attributed the resistor tombstoning we encountered to the presence of solder mask under the components. He pointed out that even though our pc board was quite flat, its solder plating (applied to the board during pc-board fabrication by the hot-air leveling process) became molten during the reflow-soldering operation. At that point, the seam between the pad and the solder mask was no longer flat; it became a step. The edge of the solder-mask layer acted like a fulcrum as the surface tension of the molten solder hoisted the ends of the resistors off the board, creating the tombstoned devices. Elimination of the solder mask from beneath passive components would reduce this problem, something we learned in our training but didn't fully appreciate until we experienced the problem firsthand.

Over the course of this project we learned not to be so fanatical about requiring that every component be an SMD. Ultimately, we used through-hole SIMM sockets, which forced us to add a wave-soldering step to our manufacturing process. Once we added wave soldering—and thus incurred its additional cost—we could have used even more through-hole components.

In particular, we feel that the pin header we used on our project board should have been a through-hole component. As an SMD, the header uses more pc-board real estate than the equivalent through-hole part, and its basic design, with pins growing out of the top, gives vacuum-pickup placement machines difficulties—it's like trying to pick up a porcupine with a vacuum-cleaner hose. That's why we placed the components on our boards by hand during our prototype run.

One experiment we'd perform before putting this product into production would be to build a few more boards with the LSTTL logic replaced by functionally equivalent, advanced CMOS SMDs. Although the memory section of the board runs cool to the touch, the control section becomes quite toasty. This situation emphasizes the extreme component density SMT allows you to obtain. Many engineers have developed an intuitive sense for the number of through-hole components they can cram onto a board without creating heat problems.

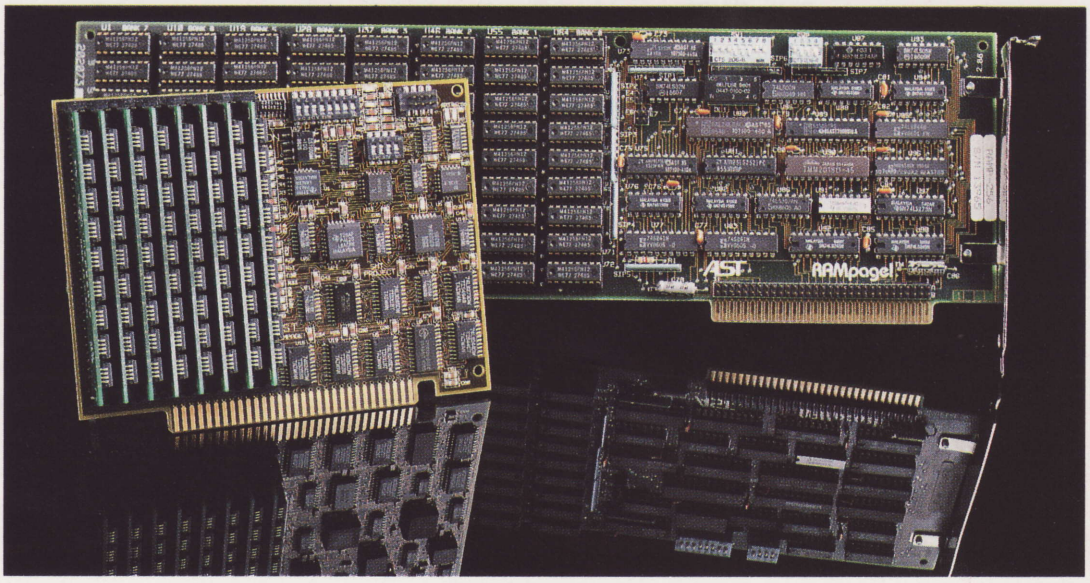
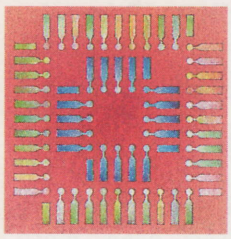


Photo by Bill Farrell, The Photo Works

The through-hole Rampage! memory card from AST Research (rear) dwarfs EDN's SMT project board, but both boards have equivalent capabilities and memory capacity.



SMT invalidates that intuition and increases the need for thermal simulation.

Goodbye to tradition

Seat-of-the-pants thermal management isn't the only tradition SMT crumbles. SMDs' small size and faster speeds put wire-wrapped breadboards on the road to extinction because device manufacturers do not design SMDs to be socketed. Socketing goes against the SMT philosophy of smaller and less expensive and introduces extra impedance that can slow or distort the high-speed signals SMDs can produce. If you start designing SMT assemblies, you should become accustomed to the idea of pc boards as breadboards. That's the only type of assembly that will give you a true picture of your design's performance.

We find the increasing availability of analog and digital simulation software on CAE workstations quite opportune because it coincides nicely with SMT's growing popularity. With a pc board serving as your breadboard for SMT assemblies, you'll want to simulate the circuits on your board to give you confidence in your design before committing it to fabrication, because SMT pc boards are tough to patch. Cutting and jumping circuit traces to fix design errors in a prototype circuit board doesn't work very well in SMT's world of fine-line circuit-board traces and small component lead pitches.

As more designers turn to SMT to create products, we foresee the need for closely linked CAE workstations, prototype and production placement machines, fixturing equipment, and board-test ATE. Few engineers will tolerate the constant manual transfer of design information from one computer-based system to the next that seems to be the norm today. As we discovered during this project, manual information transfer between computerized systems lessens both speed and accuracy. We see this situation as quite an opportunity for a large company or group of companies to wrap the entire SMT-assembly development process, from design to manufacture, into one neat package.

For most companies, SMT isn't an end unto itself; the technology is simply a tool for you to put into your toolbox along with data books, soldering irons, standard logic parts, ASICs, and μPs. Even though SMT is more than 20 years old, wide-scale use awaits further refinements in components, design tools, and assembly automation that will make the technology a truly universal engineering tool. As with any engineering tool, the trick is to know when, and when not, to use it.

EDN

Acknowledgment

Many, many people contributed to the success of EDN's SMT project. We appreciate all their contributions. A few people made outstanding contributions. We especially thank Art Lindsay and the CAD instructors at Cadnetix, John Maxwell at AVX, Dr Charles Hutchins at Texas Instruments, and Mitch Killmon at Hewlett-Packard.

No matter how many machines and systems an engineer has for aids, people still make the difference between the success and failure of a project.

For more information . . .

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