EDN's Hands-On
SMT Project—Part 3

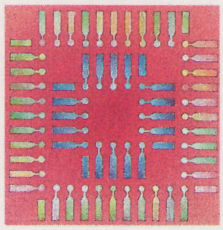
CAD and surface-mount technology

With the parts list completely converted to SMT components, we were ready to tackle the design of our SMT project board using a high-end, pc-board CAD system. What we learned about the features required to perform CAD-based SMT design applies to all CAD systems from low-end, PC-based tools to the most expensive workstations.

Lead pitches on SMT components have reached 50 mils today and will drop to 40 or 25 mils tomorrow, so you can't readily use tape, rubylith, and an X-acto knife to design complex, manufacturable SMT pc boards. The fine-line geometries used on SMT boards make the use of a CAD system almost mandatory. Many CAD vendors claim that their products support SMT design, but you should be aware that these design tools have varying levels of capability. Our encounter with SMT pc-board design demonstrates the features you should look for in a pc-

Steven H Leibson, *Regional Editor*

Illustration by Michael Young

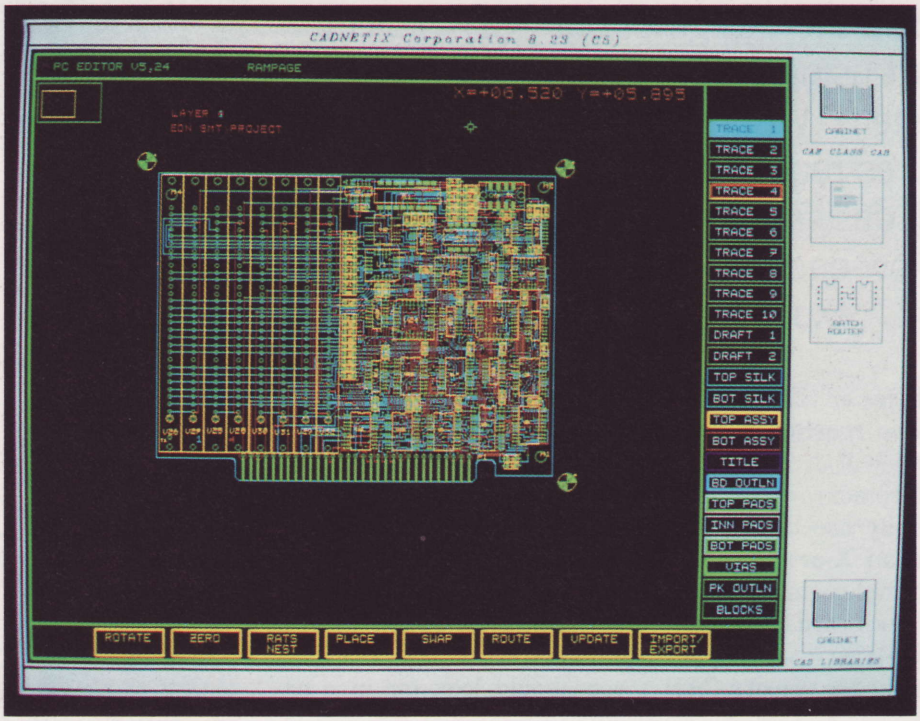


board CAD package.

Our SMT memory board, although moderately complex, does not push the limits of pc-board fabrication or SMT assembly processes. Nevertheless, it allowed us to experience and solve many problems associated with the technology. We spent extra time and effort relaxing clearances between traces and pads on the board to make our design as manufacturable as possible.

Picking out the patterns

Before sitting down at our CAD workstation, we needed to select the pad patterns. SMT Plus had given us an excellent set of patterns from the class we attended (**Ref 1**), and we used the SOIC pad patterns provided by that company. We also used recommendations from a few other sources.



After weeks of development, our pc-board plot tape was ready to ship to the fabricator. Our experiences in generating this image helped us understand what features a CAD system should have to facilitate SMT board design.

AVX provided us with an application note (**Ref 2**) that contained pad patterns for passive chip components. We discussed these recommendations with John Maxwell at AVX and inspected test boards that AVX had built to test pad configurations for passive SMDs. Because of the exhaustive testing AVX performed on these passive-component pad patterns, we decided to use AVX's recommendations for our 1206 chip capacitors and resistors.

We also received pad-pattern recommendations from Dr Charles Hutchins at Texas Instruments, who agreed to help us assemble our boards. Dr Hutchins manages TI's SMT laboratory and supervises the company's SIP-memory-module assembly line. His pad recommendations are based on experiences with these two operations. TI's SIP manufacturing line uses large quantities of PLCC memory devices to build memory modules, so based on that experience, we decided to use Dr Hutchins's PLCC pad patterns, which are published in **Ref 3**.

A few of our components were odd enough that none of our sources offered pad recommendations for them. These devices included Molex's surface-mountable SIMM (single-in-line memory module) socket, Augat's Alcoswitch SMD switches, Dallas Semiconductor's DS1000 silicon delay line (in the SMD conversion of an 8-pin DIP), and Burndy's pin header. Fortunately, these products' manufacturers supplied pad patterns for their devices in the component data sheets. Having no alternatives, we adopted the manufacturers' recommendations.

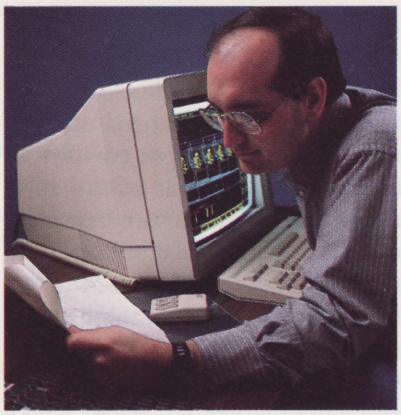
Specs for ghost components

Two critical geometries did not come from component specifications but from our pc-board fabricator. We determined trace/space widths and via sizes for our board through talks with the Tektronix Printed Circuit Board Manufacturing Division. We selected Tektronix as our pc-board vendor based on a recommendation made by Cadnetix. In addition, Tektronix had already developed expertise in working with the plot and drill tapes generated by Cadnetix systems.

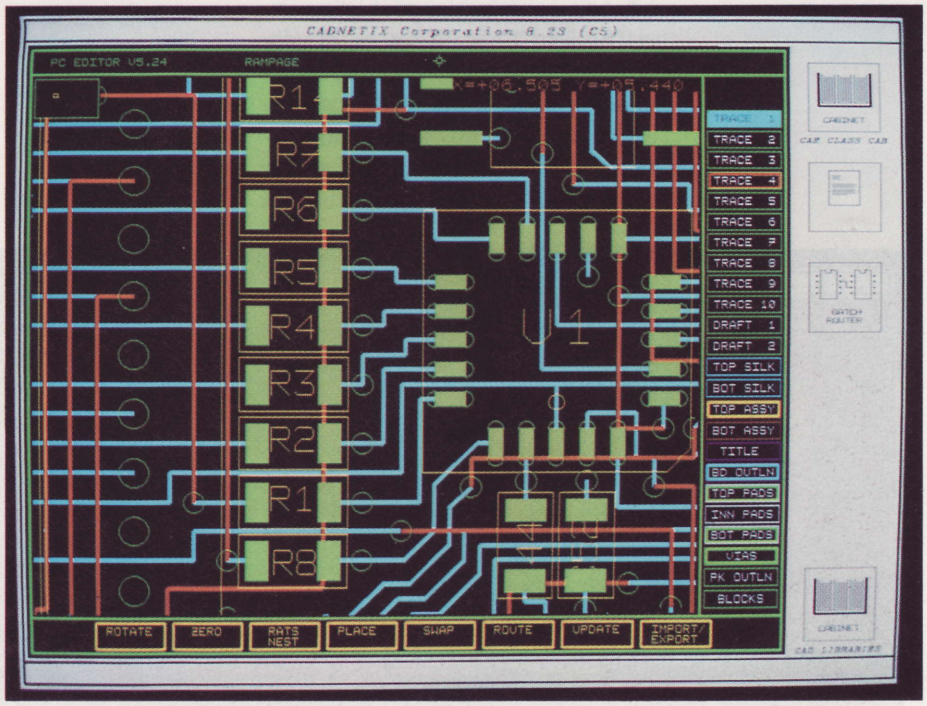
Tektronix provided our initial design rules at a meeting held on

November 12, 1985. Tektronix representatives said their process could produce 2-mil lines but that a 6-mil-trace/6-mil-space rule was more routine and that boards using an 8-mil-trace/8-mil-space rule are easily fabricated. We decided to use 8-mil spacing if possible to enhance our board's manufacturability.

We also discussed minimum via sizes at that meeting. Vias often seem insignificant on through-hole designs because holes for the component pins provide many of the vias and because through-hole components are much larger than vias. However, complex, multilayer SMT boards need lots of vias to interconnect layers because there aren't any component pins to do the job. We settled on a design using a 40-mil pad diameter and a 28-mil hole. Although we didn't realize it at the time, the 40-mil via would become the limiting factor for our design, preventing us from designing a 4-layer board and forcing us to use six layers.



Because hand-drawn schematics allow an engineer freedom to draw any kind of symbol for a component, EDN editor Steve Leibson took extra care transferring the Rampage! schematic into the less-flexible CAD environment.



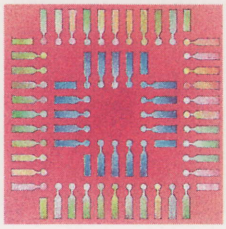
The hierarchy of CAD-based design

When you design a pc board using CAD tools, you start small and work your way up a hierarchy. You can't draw a schematic until you have built the files containing the descriptions of the components you'll use. On the Cadnetix system, component files contain electrical information about the device and designate an associated shape file. Each shape file includes a list of individual pads used to build that shape. A pad represents the lowest, atomic level of a component. The Cadnetix system stores component, shape, and pad files in separate libraries.

Although Cadnetix supplies libraries of pads, shapes, and components, we built our own files for two reasons. First, none of the Cadnetix pads or shapes matched the recommendations we planned to use. That doesn't mean the Cadnetix designs won't work. It simply means we preferred to use other patterns for reasons listed above. In addition, some of the components on our board didn't exist in the Cadnetix libraries, so even if the Cadnetix pad patterns had matched the recommendations we planned to use, we would still have built at least a few components.

As our first step, we built our pad library containing all of the pad designs we would need on our board. We initially created rectangular pads for the PLCCs because that's what all the recommendations specified. Rectangular SMT pads are extremely easy to draw on the Cadnetix system, requiring less than a minute to make. However, when we progressed to building shapes from these pads, we ran into problems when we tried generating PLCC patterns.

Manual editing of the automatically routed traces enforced the special design rules that SMT Plus provided to us. As an example, we moved all of the traces connecting to the resistors so that every trace entered the pad at the same point. The Cadnetix autorouter does not use diagonal lines, so we added them where we wanted additional clearance between traces.



At each corner of the PLCC, a vertical column of pads meets a horizontal row of similarly shaped pads (**Fig 1**). If the pads are rectangular, the closest corners of the pads at the end of the rows and columns come very near to each other, closing off possible routing channels. In the interest of maximizing the routability and manufacturability of the board, we decided to round the ends of the individual PLCC pads. That's when we ran into a problem.

The PLCC pads we originally built measured 70×25 mils, so we needed 25-mil diameter half-circles at each end of the pad. Although the Cadnetix pad editor allows you to use arcs and circles to construct pads, it only accepts arc radii in integer mils. A 25-mil diameter pad has a 12.5 mil radius, so we couldn't build exactly the pad we wanted. We finally settled for a 70×26 mil pad (**Fig 2**). The 26-mil pads on 50-mil lead-pitch spacings left 24 mils between pads: exactly enough room for one 8-mil trace to run between the pads with eight mils of clearance on either side of the trace.

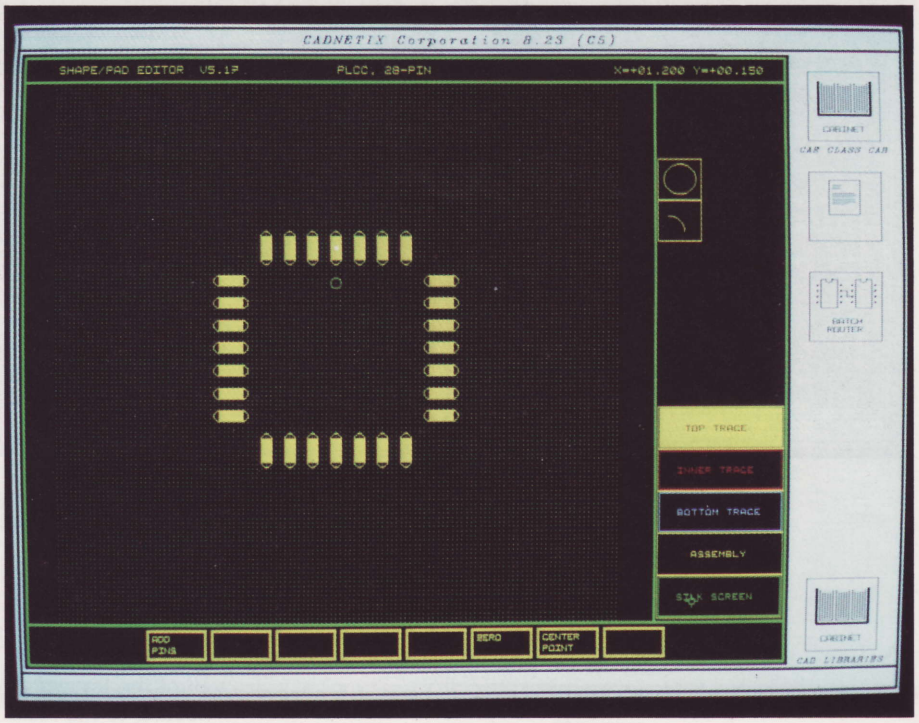


Fig 1—The four-sided PLCC pad pattern forced us to reconsider our pad design. At the intersections of the horizontal rows and vertical columns of pads, the corners of rectangular pads come too close to each other to allow us to route a trace between the corner pads.

Another problem we encountered when building component shapes was the inability of the Cadnetix system to treat the pc board's solder mask as a separate layer. The system assumes that the solder mask starts at the edge of the pads and covers the rest of the board. For through-hole boards, that assumption doesn't usually pose a problem. But for our SMT project board, we wanted the areas beneath our 1206 capacitors and resistors clear of solder mask.

SMT Plus recommends this approach because the solder mask can sometimes bubble, blister, or fold during pc-board fabrication. If a solder-mask imperfection occurs beneath a passive component, it can force the device off the board and create an open circuit. Passive components are especially susceptible to this manufacturing defect because passive-SMD bodies sit flush against the pc board. Active devices like transistors and ICs avoid this problem because they tend to stand up off the board on their leads. In addition, if any of the solder mask encroaches on an SMT pad, the pad becomes unsolderable, so we wanted to put around each pad a 10-mil moat that would be clear of solder mask.

After several attempts at workaround solutions to controlling the solder mask, we abandoned the effort and accepted the solder mask created by the Cadnetix system; we relied on Tektronix to give us a well-controlled solder mask, which the company did. We could have manually edited the solder-mask layer generated by the Cadnetix system after the board was finished. However, this post-processing step would be invalidated every time we went back and moved a component on the board layout. We deemed this procedure more trouble than it was worth, because we had selected a pc-board vendor and knew what the vendor could accomplish.

A similar problem occurred when we tried to find a way to prevent the Cadnetix router from

placing vias beneath passive components. For pc boards that will pass over a solder wave to solder through-hole components to the board, you'll sometimes see manufacturing defects occur when solder splashes up through a via and becomes trapped beneath a passive component. If you're lucky, the solder creates a permanent short circuit that's easy to find, but if your luck isn't too good, you'll have an intermittent short.

Passive SMDs are especially susceptible to this sort of manufacturing defect, again because the components sit flat on the board. Cleaning systems don't always remove solder and other debris from beneath these SMDs. The best solution to this problem is to exclude vias from beneath all passive SMDs.

On the Cadnetix system, our solution to this problem involved dropping small bits of trace on an unused layer underneath each passive component. The automatic router treats these bits of trace as barriers and will not place a via through one. Because we didn't plan to fabricate the layer containing these bits of trace, this technique created only one side effect: If we moved one of the passive SMDs, we had to remember to move the associated via-blocking bit of trace. Because we usually left that otherwise-unused layer undisplayed, we often forgot to move the associated bit of trace when we moved a passive SMD. This solution also points out the need for many additional layers when designing SMT boards. SMT Plus claims you need 15 CAD layers to design a 6-layer SMT board to allow for silkscreens, solder screens, land masters, pad masters, front- and back-side component locators, and computer-aided-manufacturing data.

With all the preparation required to create the component, shape, and pad libraries, schematic entry became the smallest part of this project phase. The Cadnetix schematic editor includes one feature that certainly eased our schematic entry: buses. Our design has six buses ranging in size from five to 20 bits. We saved quite a lot of time because it's much easier to route a single 20-bit bus around a schematic than 20 individual wires. This feature was especially useful in drawing the memory array (**Fig 3**); we wired the address and data buses to the SIP memory modules in only a few minutes. The bus representation also makes the schematic more understandable by reducing clutter.

After entering the schematic, we were ready to place the components on the board. A good component placement makes a board easy to route, and a bad placement can make a board unroutable. AST's Rampage! posed a tough routing problem. Our design's six buses link components all over the board, causing trace congestion in several places. We tried several placements, and one of Cadnetix's benchmark experts, Vinnie Magnifico, tried his hand as well. We tested our trial placements by submitting each one to the route engine and stopping the routing after 10 passes. Then we selected the layout with the highest percentage of completed connections.

When we were ready to route the traces, we encountered a problem the Cadnetix automatic router has with SMT boards.

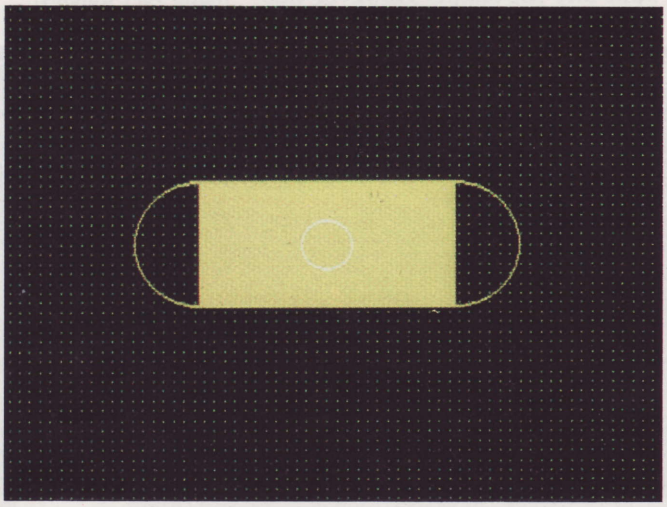
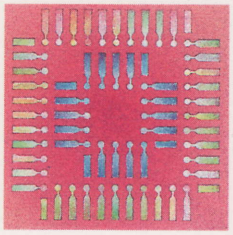


Fig 2—We solved the PLCC-pad problem (illustrated in **Fig 1**) by rounding the ends of the pad, but that forced us to change the pad's width from 25 to 26 mils. The Cadnetix pad editor only allowed even diameters for circles and arcs.



Cadnetix has a special negative-layer automatic router, which connects a selected negative layer to every pin that pierces the layer and that's supposed to connect to the selected node (that is, power or ground). That approach works great for through-hole components, but SMDs don't have any pins. To connect an inner layer to an SMD on the Cadnetix system, you must manually generate a via and route a short trace between that via and the SMD's pad on the board's outer layer. The Cadnetix automatic routers couldn't perform this task. For this reason, Cadnetix recommends that you create SMD shapes with stringers leading from the pads to vias built into the shape. However this solution consumes additional real estate and limits your flexibility in dropping vias where needed.

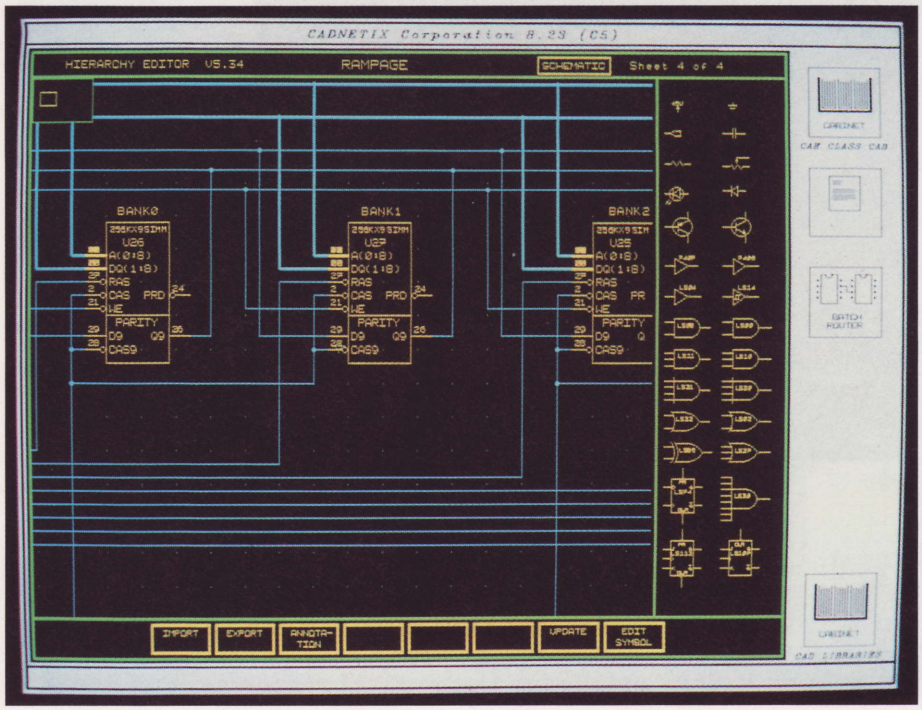


Fig 3—This part of our schematic shows the 256k×9-bit SIMM modules and the associated buses. Together, the memory address and data buses represent 17 signals, but on the schematic we drew only two lines. The shorthand notations for the SIMM and the buses allowed us to draw the memory-array portion of the schematic very quickly.

Instead, we chose to make all power and ground connections to the SMDs manually. We dubbed this procedure "stapling," because it affixes the components to the power and ground layers and makes them hard to move. If we wanted to move a stapled component, we had to delete the short power and ground traces plus the associated vias, move the component, and then restaple the device. This limitation illustrates that systems supporting both through-hole and SMT design don't necessarily allow you to create SMT boards as easily as through-hole boards.

About this time, we became concerned because the surface-mountable SIMM sockets had not arrived from Molex. We contacted the company and discovered that the other customer requesting this part was no longer interested in the SMD version. As a result, Molex had not created the tooling for this product but offered to build us enough surface-mountable sockets for our project. Instead, we switched to the company's through-hole SIMM sockets because we preferred to use a standard product.

We submitted our final layout to the route engine and let the system work on the board overnight. Initially, we instructed the route engine to complete the board using only two signal layers. The additional layers for power and ground would produce a 4-layer pc board. When we returned the next morning, the route engine had hit an impasse. It had routed traces for two hours but added no more after that time. We retrieved our file from the route engine and discovered the reason for this problem: Those 40-mil vias choked off all of the routing channels.

As an experiment, we tried routing the board with four signal layers, which would result in a 6-layer pc board. The route engine completed the entire board in less than 30 minutes. The 6-layer board didn't require nearly as many vias as the 4-layer version. Our time was running out because we were scheduled to take our plot tape to Tektronix shortly. Reluctantly, we elected to use the 6-layer board and proceeded to implement some of our SMT design rules in a manual cleanup pass.

Most automatic routers don't allow you to implement all of the

SMT design rules in the route algorithm. For example, SMT Plus recommends that each pad have only one point of entry and that the points of entry to pads for 2-lead components be balanced. Multiple traces attached to an SMD pad can drain solder from the pads during the reflow operation and in extreme cases can remove all the solder, resulting in an open joint. You plug this leak by allowing only one small trace to enter each pad. Solder draining down unbalanced traces creates a turbulence in the molten solder during the reflow operation that can drag or spin a component off its pads. We couldn't feed these rules to the route engine, so we enforced them manually after the board had been routed. Perhaps the artificial-intelligence crowd will take a crack at this problem.

We also used the manual editing pass to optimize some component placements for ease of assembly. That's when a catastrophe occurred. We were moving bypass capacitors, which turned out to be difficult because bypass capacitors were connected to all of the other components on the board via the power and ground networks. Somewhere in tracing through these extended networks, the route editor bombed and the workstation locked up, forcing us to turn off the machine while several data files were still open.

Later, we found out that the crash occurred because someone had loaded updated software into our workstation a few days earlier. We had done our layout with a down-level version of the route editor, and the new software couldn't reliably tear up and rebuild the networks in a file created by the old route editor. The bug would only surface during use of the pin-swapping feature of the editor, but we had used that feature.

The worst effect of this crash became apparent when we tried to recover. The accident irretrievably corrupted our routed-board file, and we were forced to start over again. In the heat of doing things at the last minute, we failed to make adequate backup copies of each step and had manually edited our original copy of the routed board. Because the crash

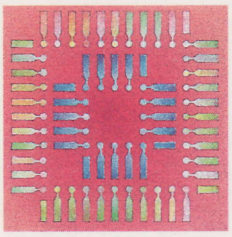
What CAD systems really need for SMT design

Characteristics you should look for in CAD systems for SMT designs include 1-layer pads, the ability to place components in the same location but on opposite sides of the board, placement and routing grids with 25-mil resolution or smaller, a wide variety of trace widths, and the ability to create irregular pads (not just rectangles and circles).

Without 1-layer pads, you can't route traces under the pads on other pc-board layers, which gives you more routing channels and makes your board easier to design. You must also have 1-layer pads, plus the ability to place components in the same spot but on opposite sides of the board, if you want to design SMT boards with components on both sides. Note that when you place a component on the opposite side of the board, the CAD system must provide some method of reversing the component shape, even if that method is simply to use a mirror-image shape you have previously created.

Although SMDs typically have 50-mil lead pitches, you need at least a 25-mil routing grid to route traces between those leads. We frequently used a 5-mil grid on the Cadnetix system and could have used a 1-mil grid if it had become necessary. Another routing-grid characteristic you might need is the ability to change grids in the middle of your work. Some areas of your board can become congested with traces, and a high-resolution routing grid allows you to run more traces through the same routing channel.

You need good control over trace widths for SMT designs. Our board uses mostly 8-mil traces, but some traces that carry power are 20 mils wide. We experimentally determined that dimension by changing the trace width until we achieved a good compromise between current-carrying capability and clearances. Finally, although most of our pads are rectangular or circular, some of the pads (like those for our PLCCs) have irregular shapes. You use irregularly shaped pads to optimize some SMD shapes for good manufacturability with a minimum of real-estate use.



occurred only two days before our trip, we went to Tektronix without a tape. The moral of this story is don't upgrade your software until the current project is done, and back up your files often, on any computer system.

A reprieve for the lucky

Our second meeting with Tektronix occurred on June 26, 1986. The lack of a plot tape became an asset because it allowed us to reassess the design rules we were using. We discussed the proper clearances between the traces and the edge of the board, the number of etch targets to use for the multilayer fabrication process, the pc-board thickness tolerances, and even the proper dimensions for silk-screen lines. However, the most important topic we discussed was the via size. We explained that the 40-mil via became the decisive factor that forced us into designing a 6-layer board. Tektronix gave us the go-ahead to use 36-mil vias with 23-mil holes.

We also discussed nomenclature targets that would help the pc-board manufacturer align the silk-screen with the pads on the pc board. Such alignment is critical because silk-screen ink on an SMT pad makes the pad unsolderable. You don't need the nomenclature targets after the silk-screen is applied to the raw pc board, so we hid them underneath some components on our board.

Of course no one told us, until it was too late, to also include solder-screen targets. These targets aid the alignment of the solder screen with the pc board in preparation for screening the solder paste. Solder-screening machines provide three degrees of freedom for solder-screen adjustment: X, Y, and θ. Without these targets, we found aligning the solder screen to our pc board to be a bit tricky.

One more time, please

We returned to Cadnetix for another try at routing the board. Because we were using a smaller via, we again attempted to create a 4-layer pc board. Our schematic remained intact after the crash, so we proceeded with component placement using a plotted copy of our original layout as an aid. We threw this placement into the route engine and left it overnight. In the morning, the board wasn't finished but the route engine was still making headway. As a hedge against another catastrophe, we temporarily stopped the 4-layer route, ran off a quick 6-layer board, and put it safely away. Then we restarted the partially

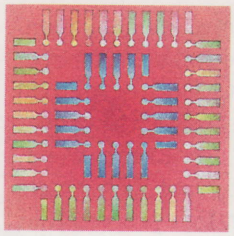
Designing pc boards on the high end

We used an $84,900 Cadnetix CDX 50000 CAD workstation to design the EDN SMT Project board. This system employs a 68020 μP as its computation engine. A bit-slice graphics accelerator allows the system to pan complex schematic and pc-board images in real time. The software bundled into the CDX 50000 includes pad, shape, component, schematic, and pc-board (route) editors.

Our system communicated over an Ethernet LAN with several other CAD and CAE workstations, a $39,900 CDX7100S file server, and a $77,000 CDX75000S route engine. The Cadnetix route engine contains a bit-slice processor designed to automatically route traces on pc boards. Although the CDX 50000 includes an automatic router that runs on the internal 68020, the route server accelerates pc-board routing by a factor of about 20.

In our opinion, the tools available on the Cadnetix workstation were up to the task of creating our project board. We created the necessary pads, shapes, and components; we were able to place these components on our board in a suitable layout; and we routed the board using a combination of the automatic and manual routers at hand.

Cadnetix recently released a major upgrade to its software. The company changed its workstations' operating system to Unix and converted all of its pc-board-design editors to that operating system. Also available with the upgrade are the VI editor, common to many Unix systems, and a technical publications package for documenting your designs.



complete 4-layer design and left it in the route engine for a week.

A week's worth of routing in a high-speed route engine using our 8-mil-trace/8-mil-space design rules may suggest that the engine doesn't work very well. In fact, a rule enforced by the software in the route engine was impeding our progress. At that time, the route engine required that the

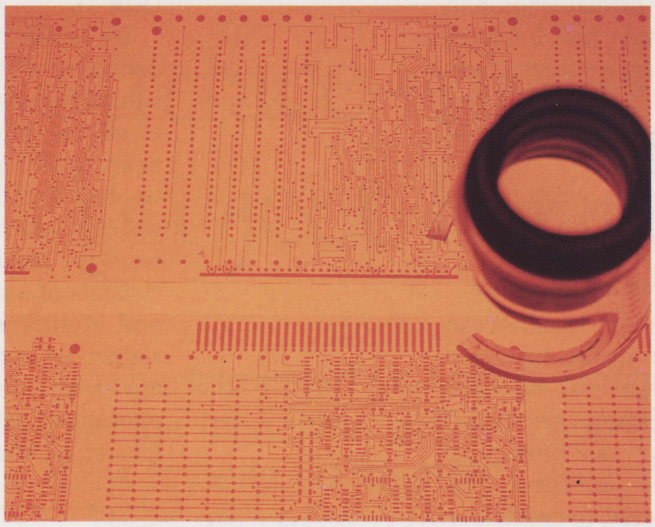


Fig 4—We caught this photoplotting error just in time. The lower plot shows a normal edge connector on the board's component side, but the pads on the upper plot are rotated 90°, thus creating a shorting bar instead of an edge connector on the circuit side of the board. The error occurred when human intervention was required to transfer information from the pc-board CAD development system to the CAD system at the pc-board vendor.

routing grid meet the following restriction:

GRID SPACING≥TRACE WIDTH+SPACE WIDTH.

In our case, because both the trace and space widths were 8 mils, we could have used a 16-mil routing grid. However SOICs and PLCCs with 50-mil lead pitches don't drop onto a 16-mil routing grid very well. We were forced to use a 25-mil routing grid to match the lead pitches of these components and still leave a channel to run one trace between leads.

Routing traces or laying track

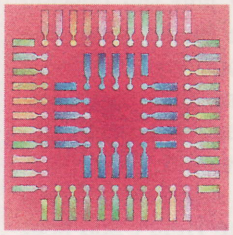
At the end of the week, the route engine continued to chug away with 27 traces remaining to route. We decided to manually add those remaining traces. At the same time, we discovered that the software engineers at Cadnetix had developed an experimental automatic router that did not impose a routing-grid restriction, so we proposed a race. We would manually add the missing 27 traces to our board while the experimental router attempted a 100% route using the same component placement. The first completed design would go to Tektronix. We felt something like a modern-day John Henry and beat the experimental router by one trace in a little less than a day. Since we used the Cadnetix system to design our pc board, the company has replaced its original automatic router with the experimental version, so we would have a much easier time routing our board today.

Before we sent the design to Tektronix for fabrication, we made two more manual editing passes. During the first, we applied the special SMT design rules we had learned to enhance the manufacturability of our pc board. We also used this pass to move traces around, evening out the spacing between them. We felt this step would further enhance the board's manufacturability, and besides, it looked better. Automatic routers don't seem to have much aesthetic sense for trace placement.

Adding vias for testability

During the other manual-editing pass, we added vias to make the board 100% testable on an in-circuit tester. Hewlett-Packard's Manufacturing Test Division volunteered to build the test fixture, to write the test program, and to test our assembled boards on its ATE equipment. We made sure that each circuit node contained one via that a test probe could reach. That technique ensured that our board would be completely testable from the back. Single-sided test fixtures cost less, exhibit higher reliability, and maintain signal integrity between the board and tester better than other fixture types (**Ref 4**).

With the design completed, our next step was to generate the plot tape for Tektronix. Although the Cadnetix system automatically



generates plot tapes in the industry-standard Gerber-photoplotter format, you must first enter an aperture list by hand. The older Gerber photoplotters use an aperture wheel to plot images, and although many pc-board fabricators now use apertureless laser photoplotters, pc-board data is still exchanged in Gerber-format files. The fundamental problem is that the Gerber-format photoplot file doesn't contain any information about the apertures, only which aperture to use. The list describing the size and shape of each aperture used (circle, square, target, etc) is a separate document.

Human intervention invites errors

Generating an aperture list can be a very error-prone task. On the Cadnetix system, we completed a form relating various pad names from our pad library to aperture wheel numbers. The system used this list to create our plot tape. Then we wrote down a list of the aperture wheel numbers we had used plus the shape, size, and orientation of each pad and later transcribed this sheet using an IBM PC and a word-processing program. We made two mistakes in this process that Tektronix caught before fabricating our board. We caught one more error when we received the photoplotted images for approval **(Fig 4)**.

We found little hiccups like this problem with the aperture list somewhat disconcerting in view of all the automation brought to bear on this project. Every time we transferred information from one computer system to the next, we were reminded of the phrase "islands of automation" that General Motors uses to describe unconnected computer systems. In any event, we blessed the second photoplot, sat back, and waited for our pc boards to arrive. **EDN**

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References

1. Leibson, Steven H, "EDN's Hands-On SMT Project—Part 1: The promise of surface-mount technology," *EDN*, May 28, 1987, pg 164.
2. Kress, Liz and Rick Charbonneau, *Solder Pad Design for Surface Mount of Chip Capacitors*, Publication No 12-83-1, AVX Corp, Myrtle Beach, CA, 1985.
3. Hutchins, Dr Charles L, *Surface Mounting Technology—How to Get Started*, D Brown Associates Inc, Warrington, PA, 1986.
4. *Testing Surface Mount Technology*, Part No 5954-5992, Hewlett Packard Co, Palo Alto, CA, August 8, 1986.